AMENDMENTS TO THE CLAIMS

Claims 1-8. (Canceled).

9. (Currently Amended) A memory device comprising:

a substrate;

a gate stack pair comprising two gate stacks formed on the substrate; a conductive contact between the two gate stacks and in contact with a doped region of the substrate;

a vertical oxide spacer adjacent to each gate stack of said gate stack pair;

a respective nitride layer overlaying and in contact with each said vertical oxide spacer and a top layer of each said gate stack, neither of said nitride layers extending to overlay said doped region; and

a respective dielectric layer overlaying each said nitride layer, the dielectric layer being spaced from each said vertical oxide spacer by said nitride layer such that said dielectric layer is not in direct contact with said vertical oxide layer.

10. (Previously Presented) The memory device of claim 9, wherein each gate stack of said gate stack pair comprises a floating gate and a control gate.

11. (Previously Presented) The memory device of claim 9, wherein each said vertical oxide spacer is between about 50Å and about 300Å in thickness.

12. (Previously Presented) The memory device of claim 9, wherein each said vertical oxide spacer is about 100Å and about 200Å in thickness.

13. (Previously Presented) The memory device of claim 9, wherein each said respective nitride layer has a thickness equal to about one half the width of each said vertical oxide spacer.

Claims 14-65. (Canceled).

66. (Previously Presented) The memory device of claim 9, wherein the dielectric layer comprises borophosphosilicate glass